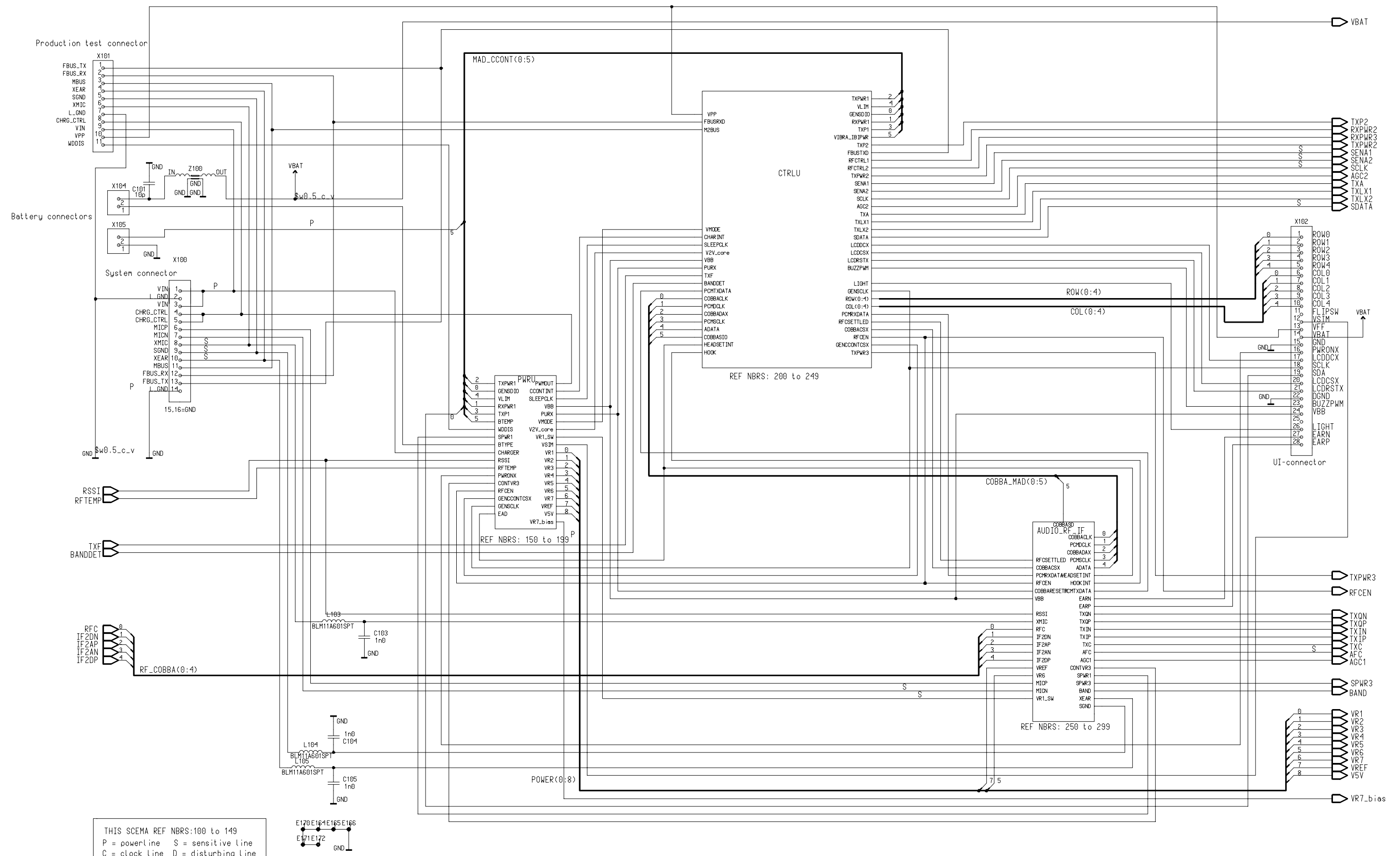
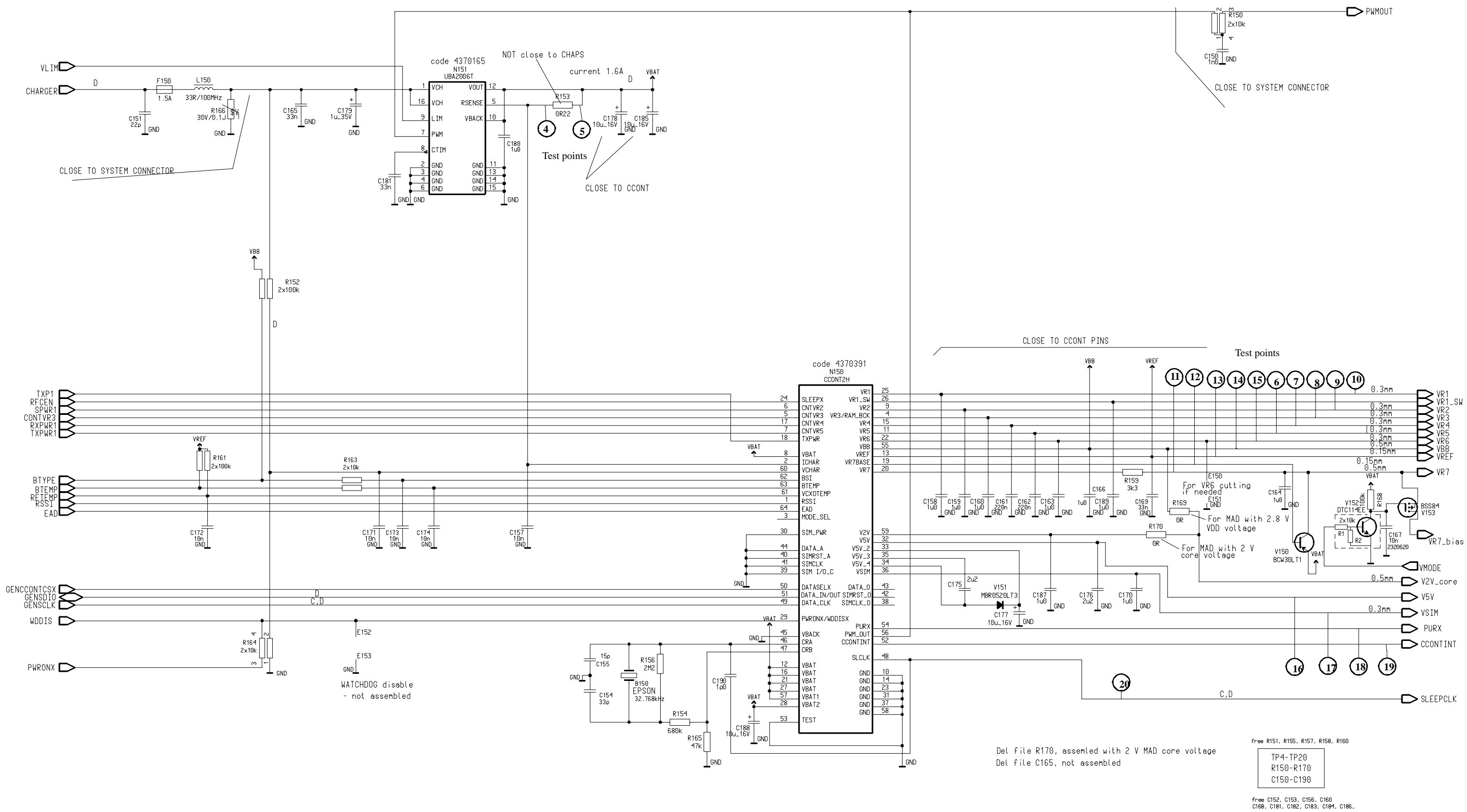


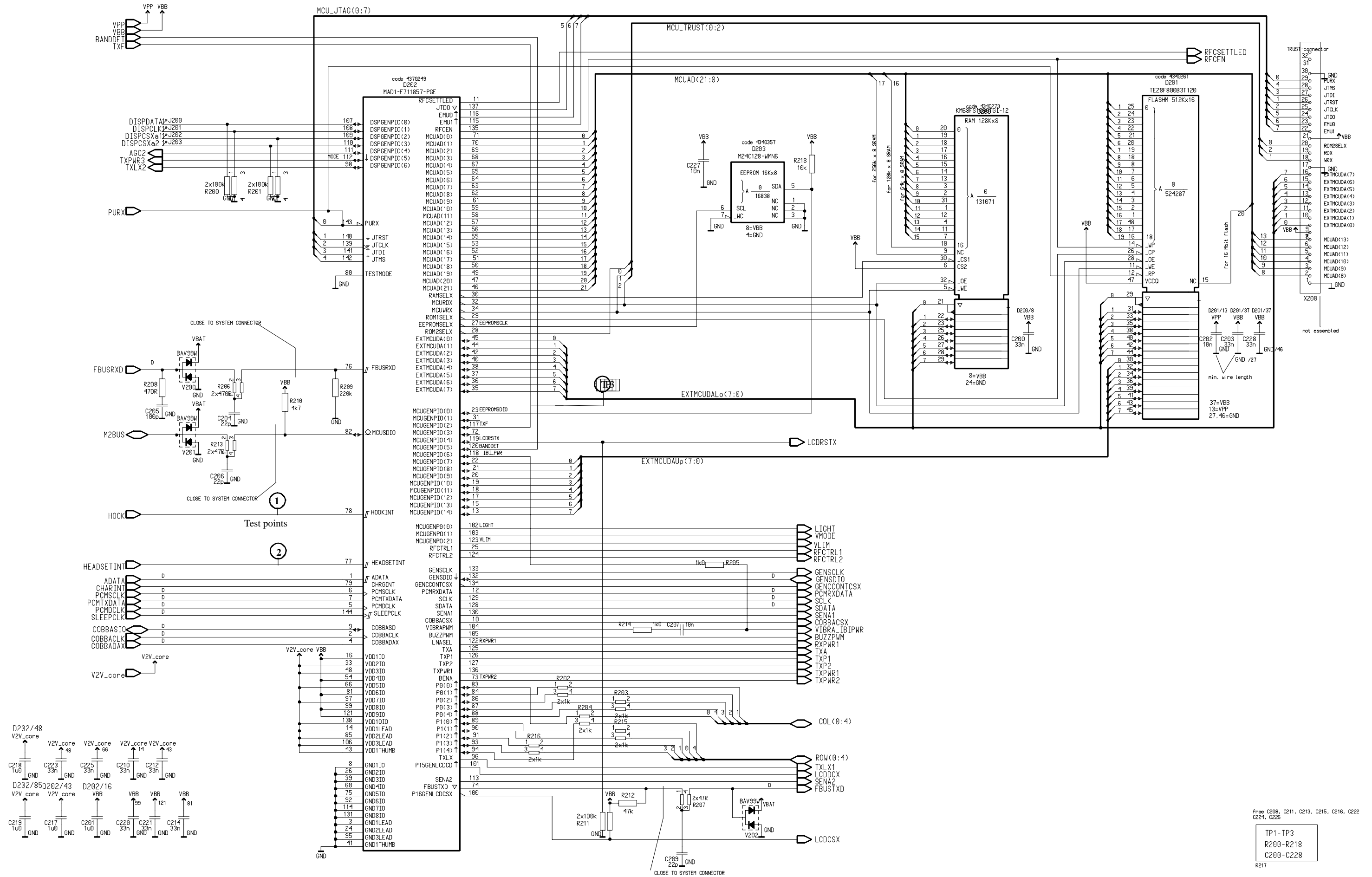
Circuit Diagram of System Blocks (Version 4.03 Edit 3)



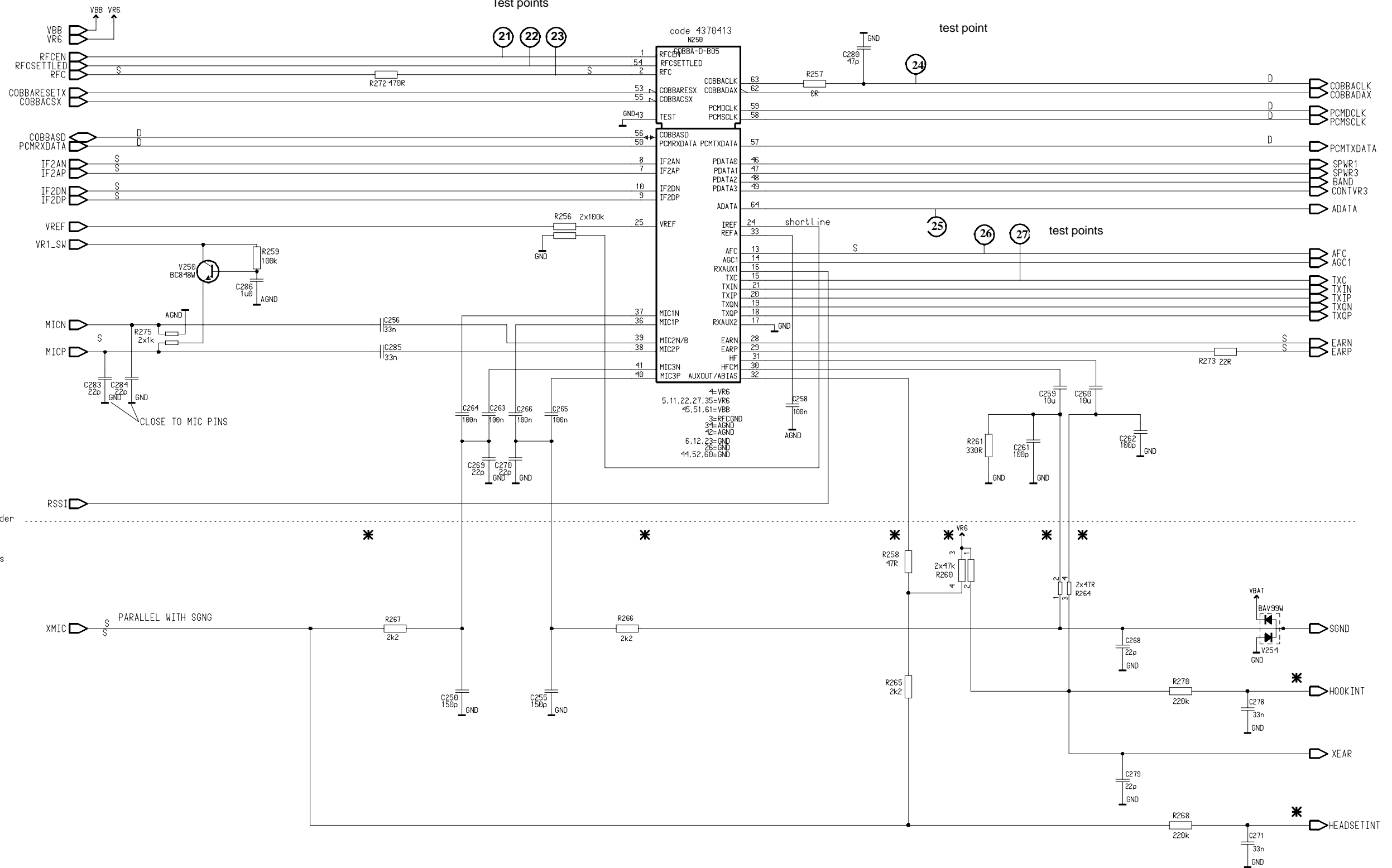
Circuit Diagram of Power Supply (Version 04.03 Edit 5)



Circuit Diagram of CTRLU Block (Version 04.03 Edit 3)

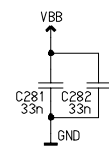
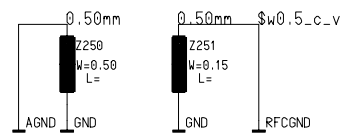
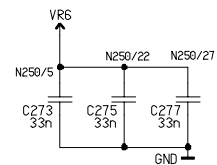


Test points



* NOT close to ESD signals

Z251 A.C.A.P to the VCX0
Z250 A.C.A.P to the N250

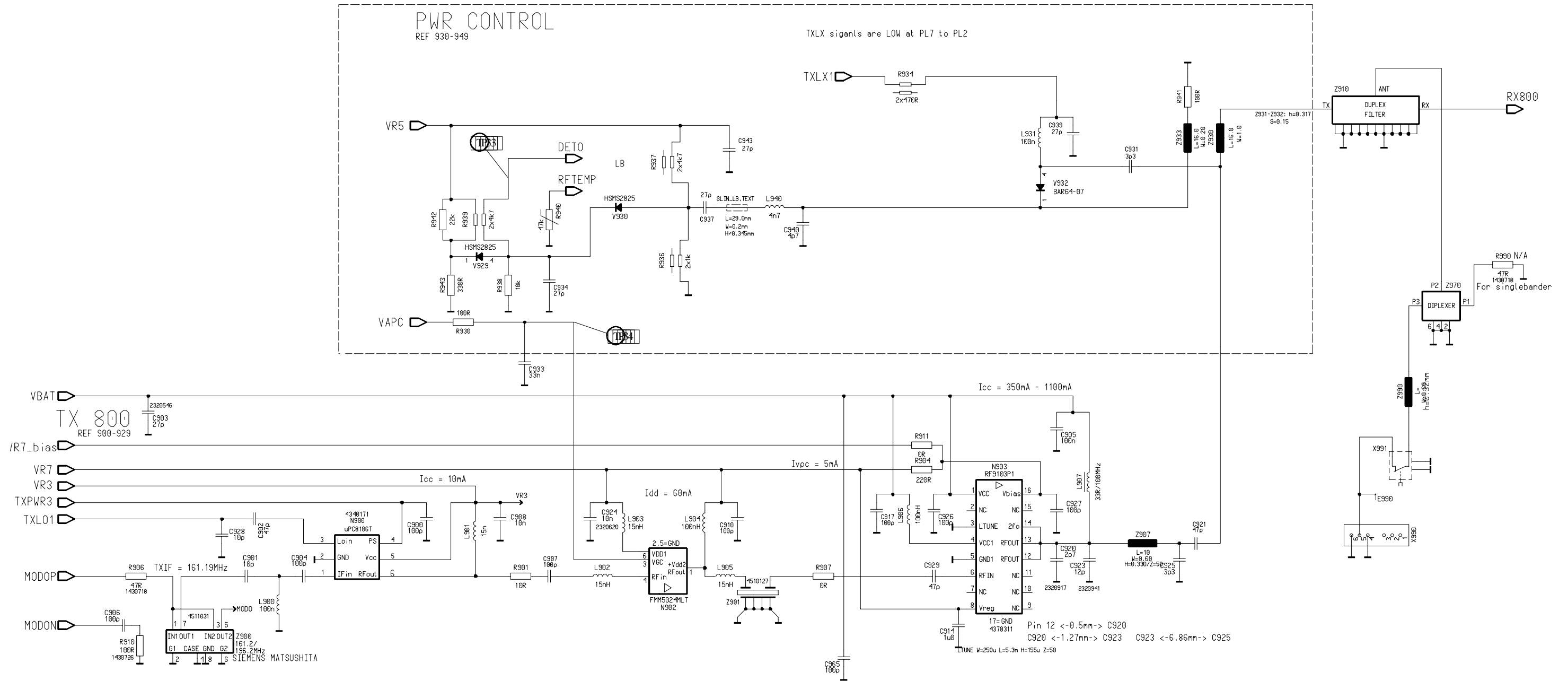


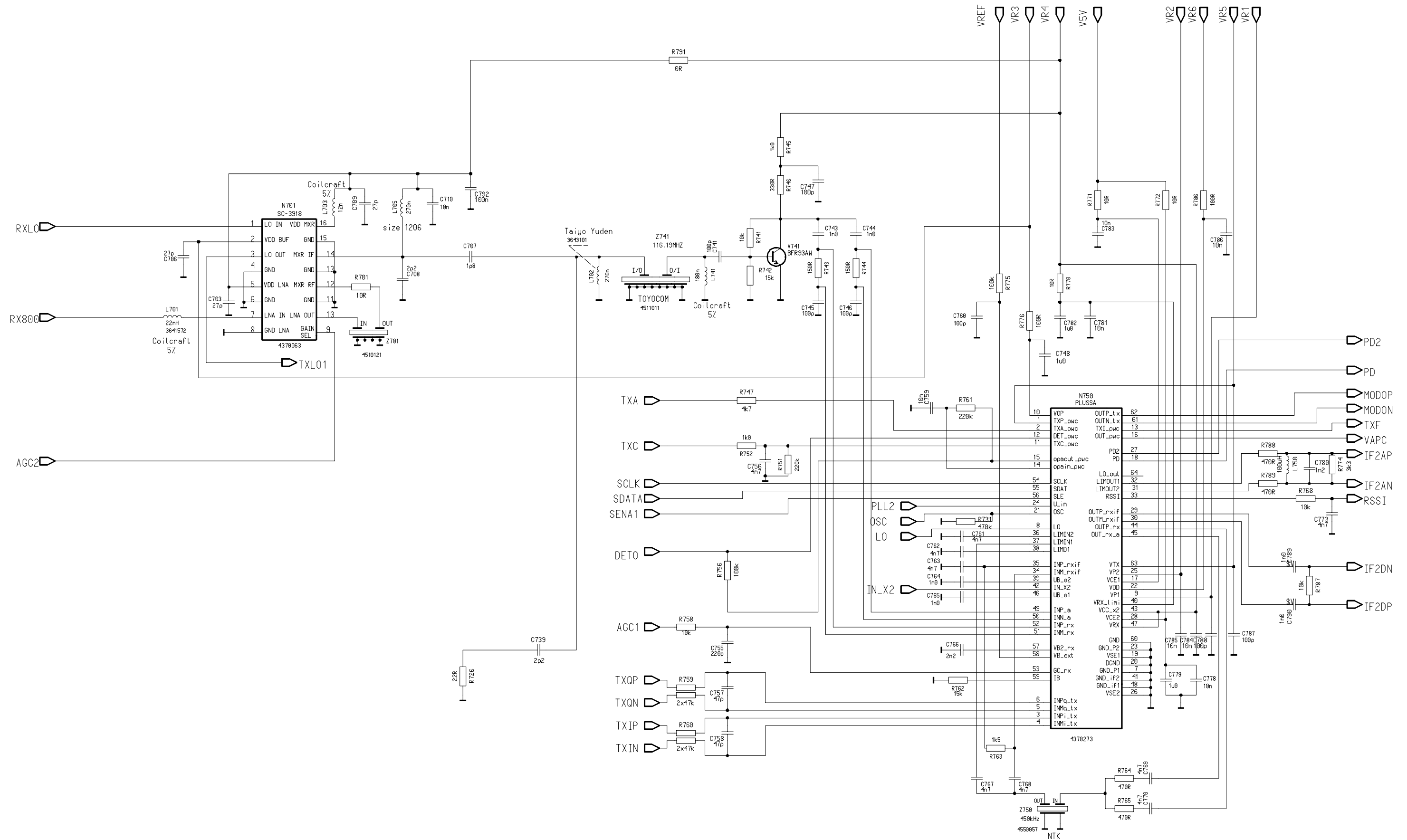
Free R252, R253, R254, R255, R262, R263, R269, R271, R274

Del file C280, assembled if needed later

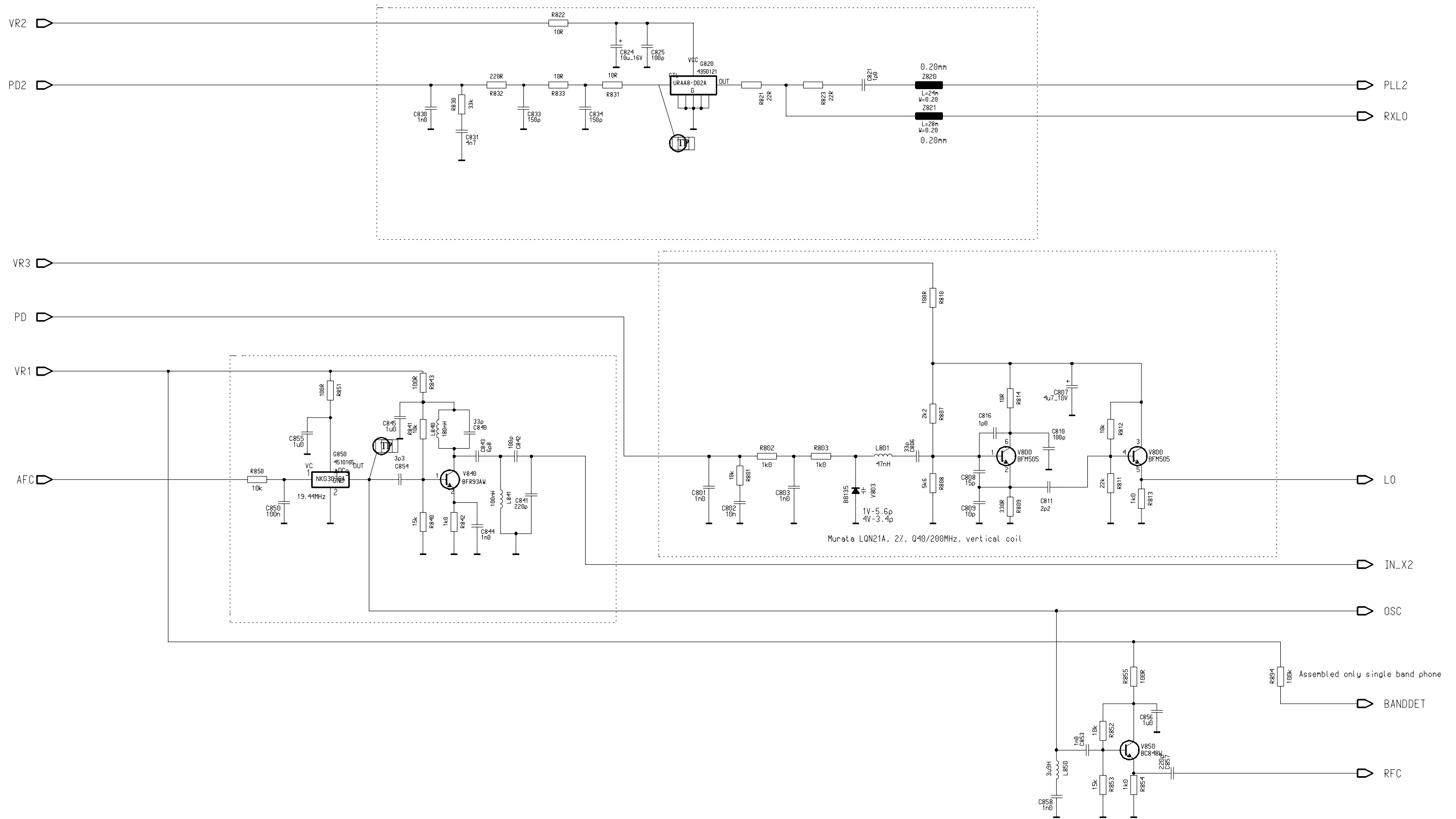
TP21-TP27
R252-R275
C250-C286

Free C251, C252, C253, C254, C257, C274, C276

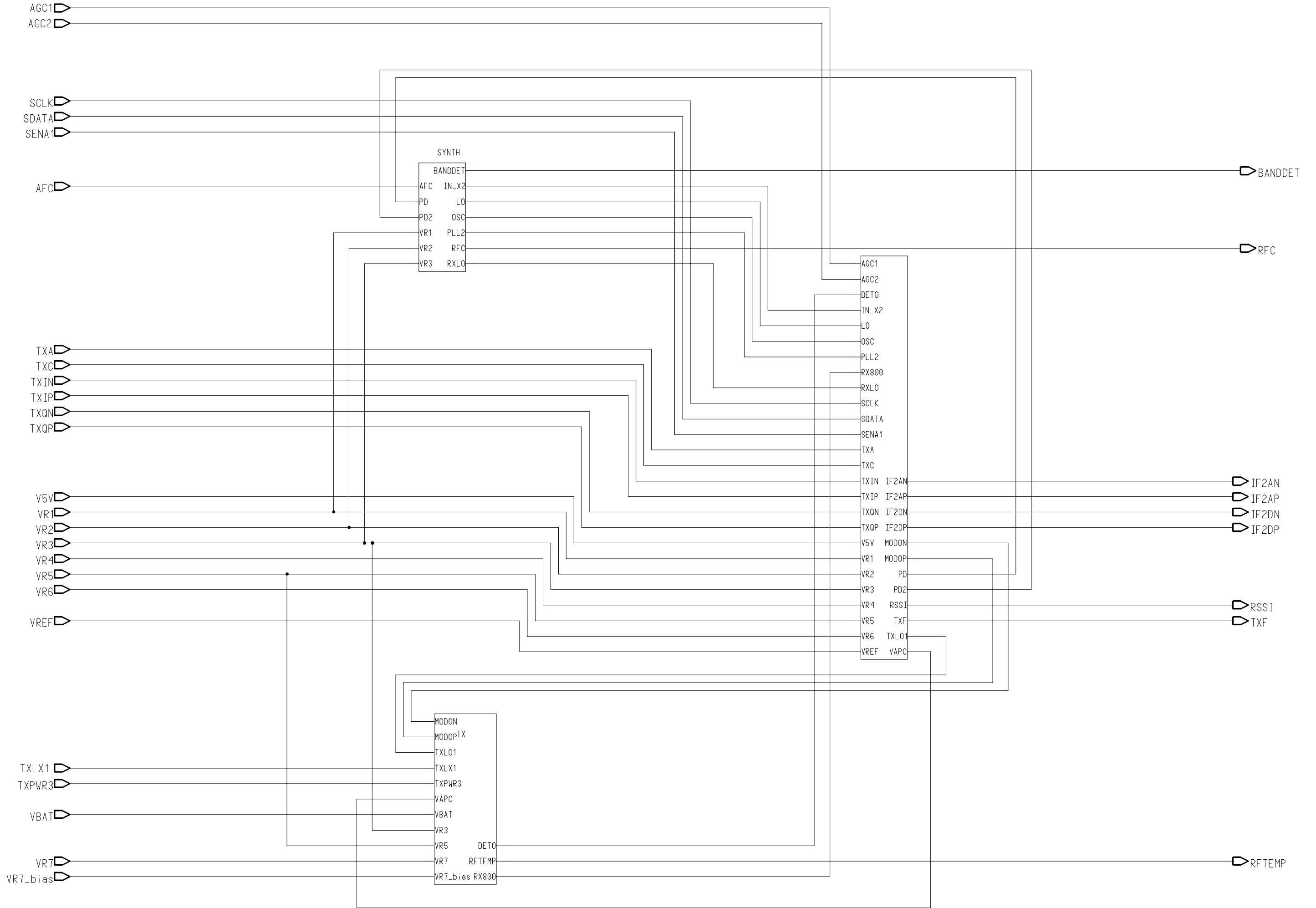


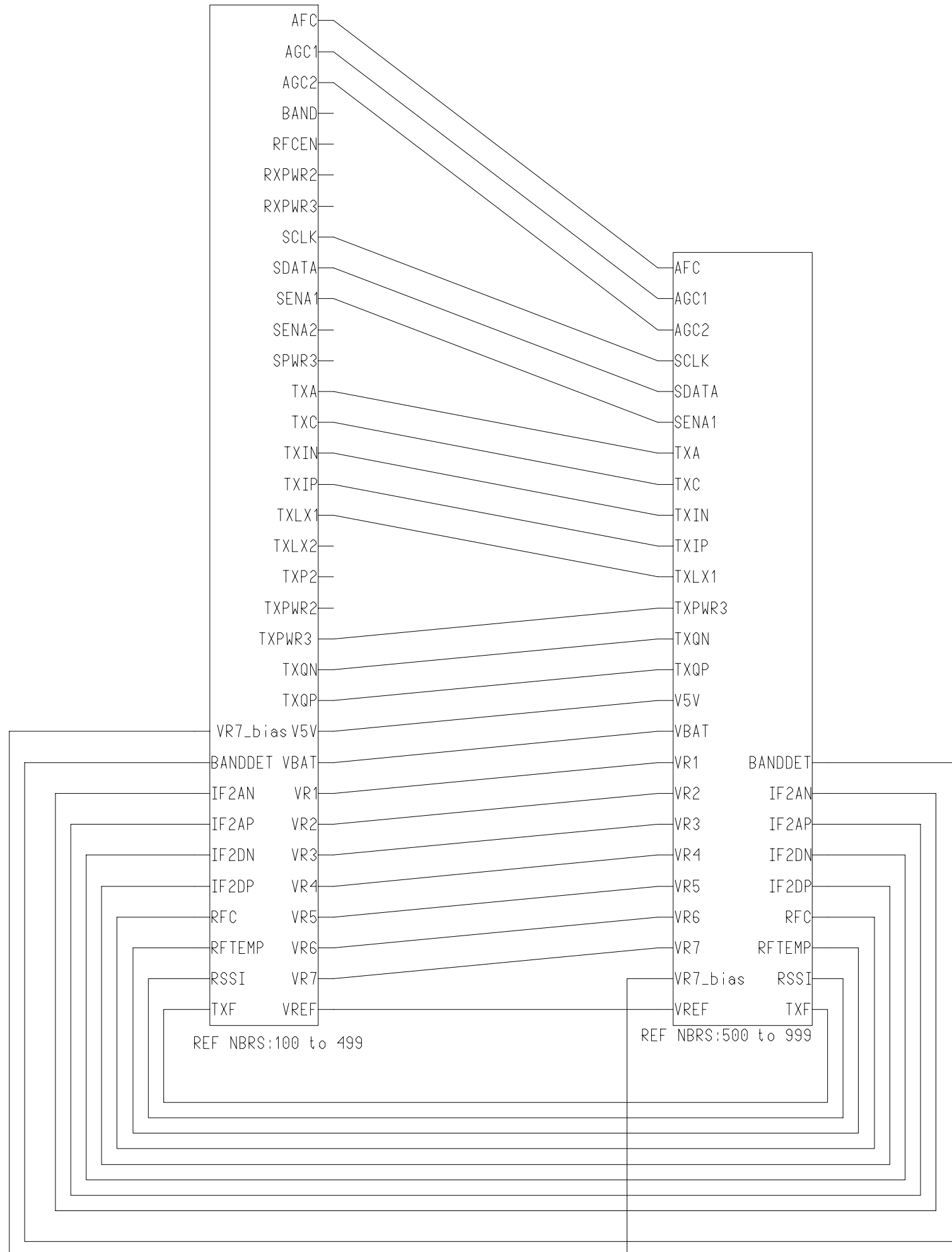


Circuit Diagram of Synthesizer (Version 4.3 Edit 3)



Circuit Diagram of RF Block (Version 4.3 Edit 2)

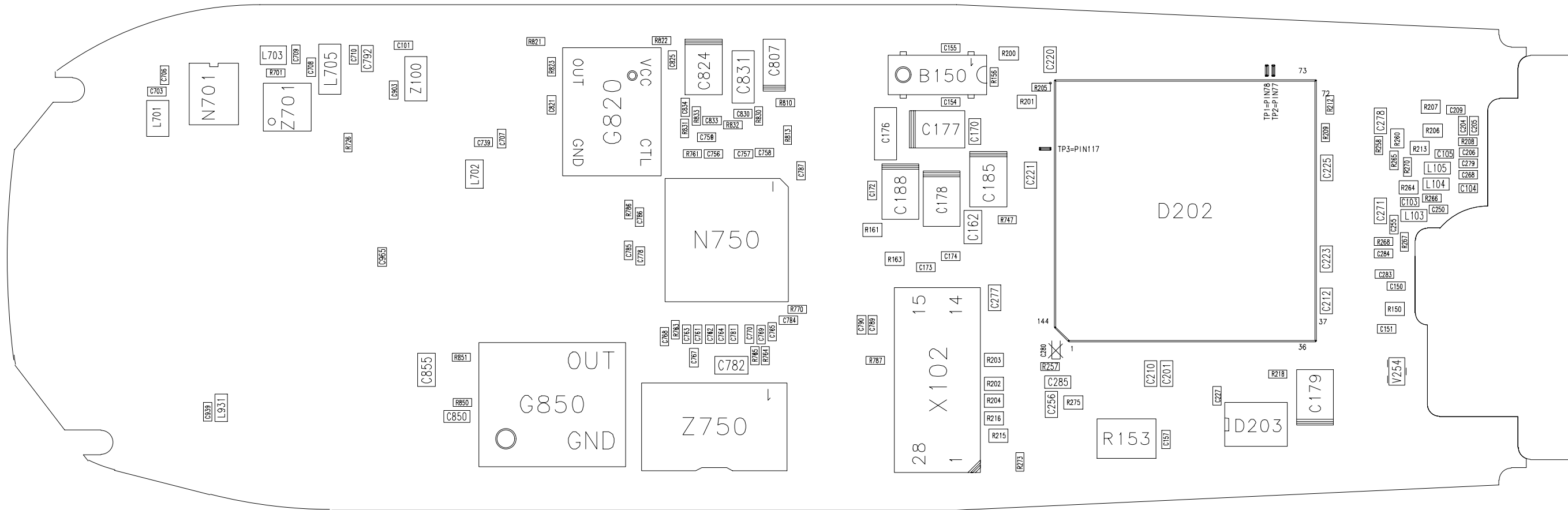




Layout Diagram 1/2 of US4RSM (Layout version 04)

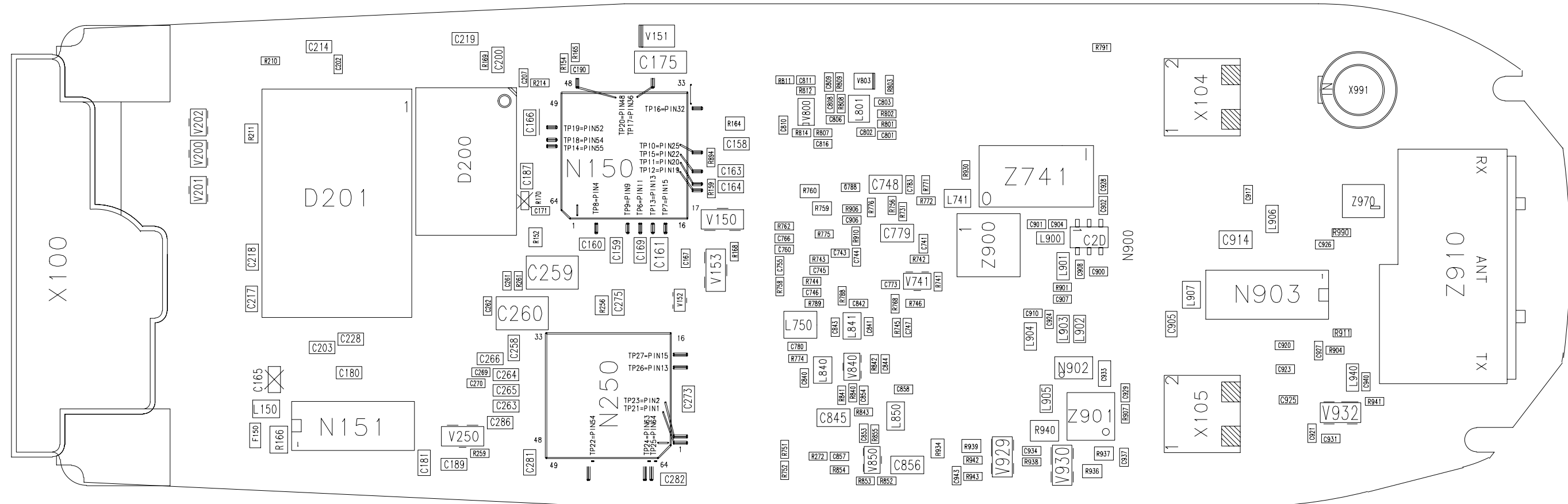
TOP

NOTE: Layout diagram has also upper band (TDMA1900) components included, which are not in actual US4U PCB. Notice this also in testpoints.



testpoint	name	condition	dc-level	ac-level
J200		Only for R&D use		
J201		Only for R&D use		
J202		Only for R&D use		
J203		Only for R&D use		
TP1, D202 pin 78	HOOKINT	Remote controlheadset	pulse active 2.8 V, non-active 0 V	
TP2, D202 pin 77	HEADSE-TINT	Headset connected	pulse active 0 V, non-active 2.8 V	
TP3, D202 pin 117	TXF	False transmission indicator	Irregular from 0 V to 2.8 V	
TP4, R153	RSense	VOUT detection	min 0V, typ 3.6 V, max 5.2 V	
TP5, R153	VOUT	VOUT detection	min 0V, typ 3.6 V, max 5.2 V	
TP30, G850 pin 3	VCTCXO	power on		typ. 0.8 V – 1.2 Vpp sinwave 19.44 MHz
TP31, G820 pin 3	CTL	active state ch 300	typ. 2.2 V	
TP32, G860 pin 3	CTL	active state ch 1000	typ. 2.2 V	

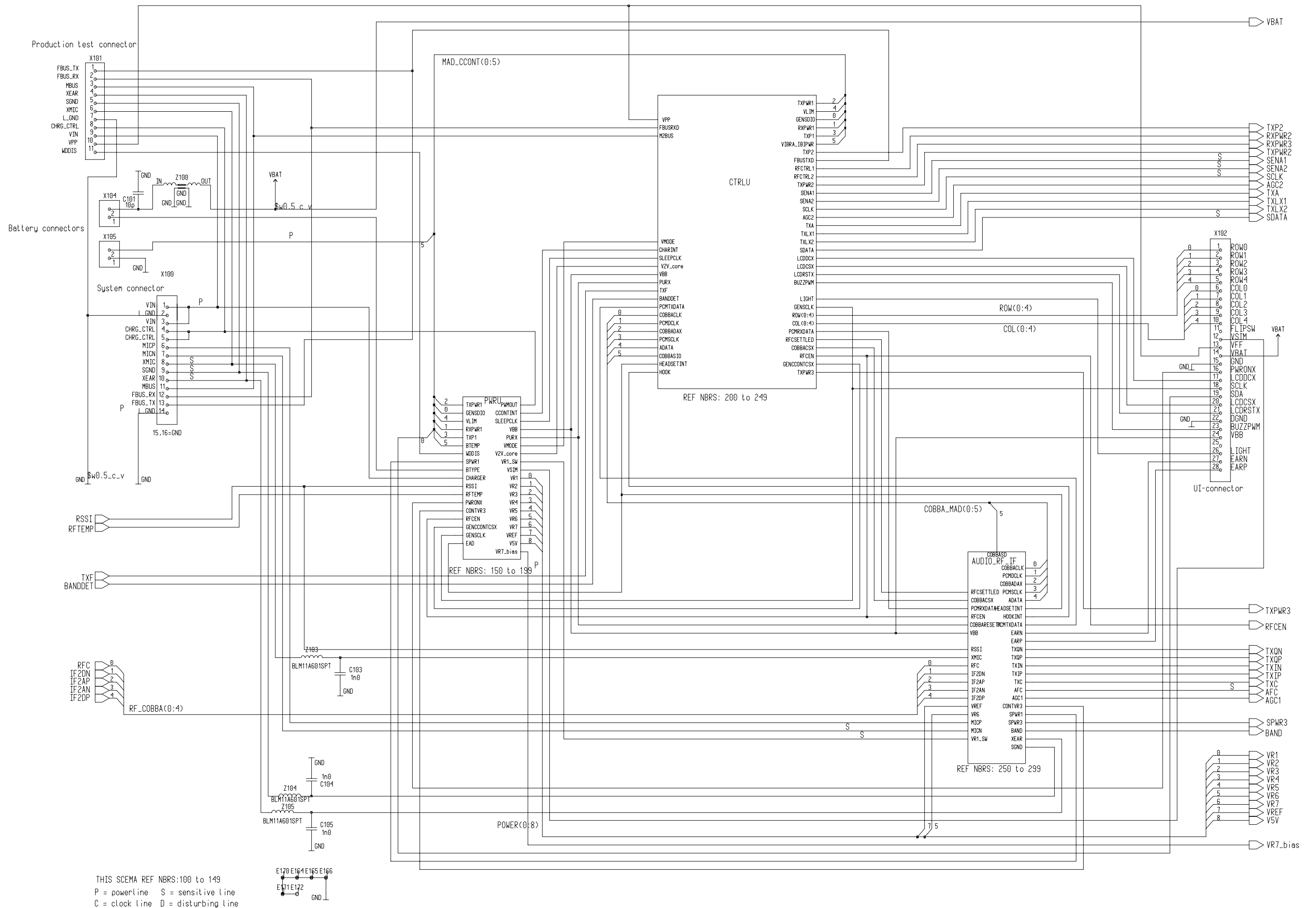
Layout Diagram 2/2 of US4RSM (Layout version 04)



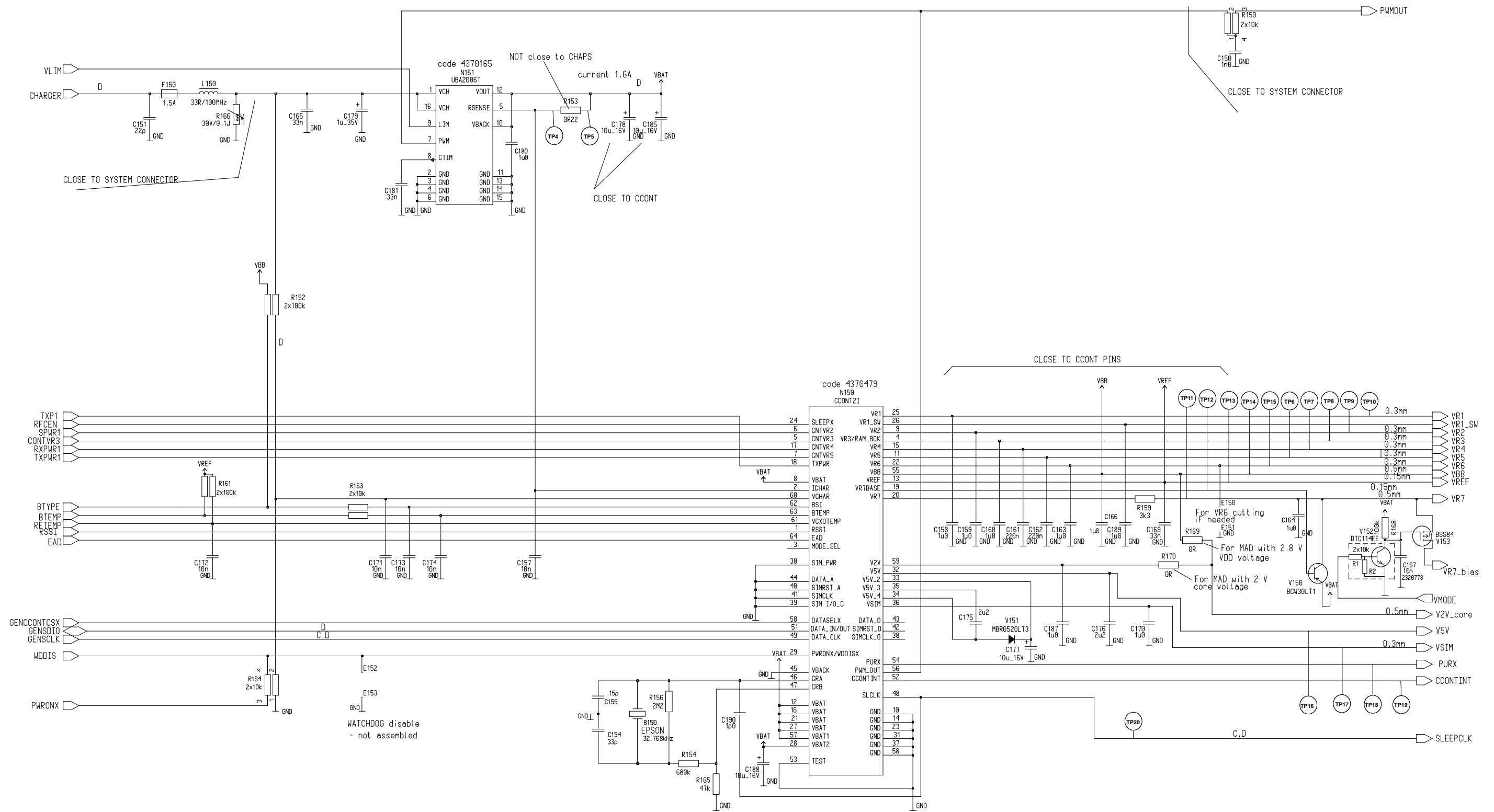
testpoint	name	condition	dc-level	ac-level
TP6, N150 pin 11	VR5	supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP7, N150 pin 15	VR4	regulated supply for RX	2.8 V min 2.7 V / max 2.85 V	
TP8, N150 pin 4	VR3	regulated supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP9, N150 pin 9	VR2	regulated supply for SYNT	2.8 V min 2.7 V / max 2.85 V	
TP10, N150 pin 25	VR1	regulated supply for VCTCXO	2.8 V min 2.7 V / max 2.85 V	
TP11, N150 pin 20	VR7	regulated supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP12, N150 pin 19	VR7BASE	VR7 regulator external transistor base current	2.8 V min 2.7 V / max 2.85 V	
TP13, N150 pin 13	VREF	ref.voltage for N150	1.5 V +/- 1.5%	
TP14, N150 pin 55	VBB	regulated supply for BaseBand	2.8 V min 2.7 V / max 2.85 V	
TP15, N150 pin 22	VR6	regulated supply for COBBA	2.8 V min 2.7 V / max 2.85 V	
TP16, N150 pin 32	V5V	regulated supply to 2GHz PLL	5.0 V min 4.8 V / max 5.2 V	
TP17, N150 pin 36	VSIM	regulated supply for flashing	3.0 V min 2.8 V / max 3.2 V	
TP18, N150 pin 54	PURX	RESET Power up/down	reset state 0 V, normal state 2.8 V	

testpoint	name	condition/type	dc-level	ac-level
TP19, N150 pin 52	CCON-TINT	Charger interrupt	pulse active 2.8 V, non-active 0 V	
TP20, N150 pin 48	SLCLK	32.768 kHz, power on	pulsed DC (0V/2.8 V)	
TP21, N250 pin 1	RFCEN	active state	pulse active 2.8 V, non-active 0 V	
TP22, N250 pin 54	RFCSE TTLED	active state	pulse active 2.8 V, non-active 0 V	
TP23, N250 pin 2	RFC	19.44 MHz sine-wave		0.2Vpp-1V pp sine-wave
TP24, N250 pin 63	COB-BACLK	9.72 MHz, active state	pulsed DC (0V/2.8V)	
TP25, N250 pin 64	ADATA	active state	pulsed DC (0V/2.8V)	
TP26, N250 pin 13	AFC	Autom.Freq.control	0 - 2.3 V, typ. 1.15 V (room temp)	
TP27, N250 pin 15	TXC	TX power control voltage	@level 10 typ.ca 0.5 V pulse @level 2 typ.ca 1.7 V pulse	
TP33, R939	DETO	active state	0.4 V - 2.2 V	
TP34, R220	VAPC	active state	0 V - 1.5 V typ.	
TP35, N702 pins 9,11,12,13,14	VR8 - VR 12	power on	nominal 2.8 V	

NOTE: Layout diagram has also upper band (TDMA1900) components included, which are not in actual US4U PCB. Notice this also in testpoints.



Circuit Diagram of Power Supply (Version 06.43 Edit 9)

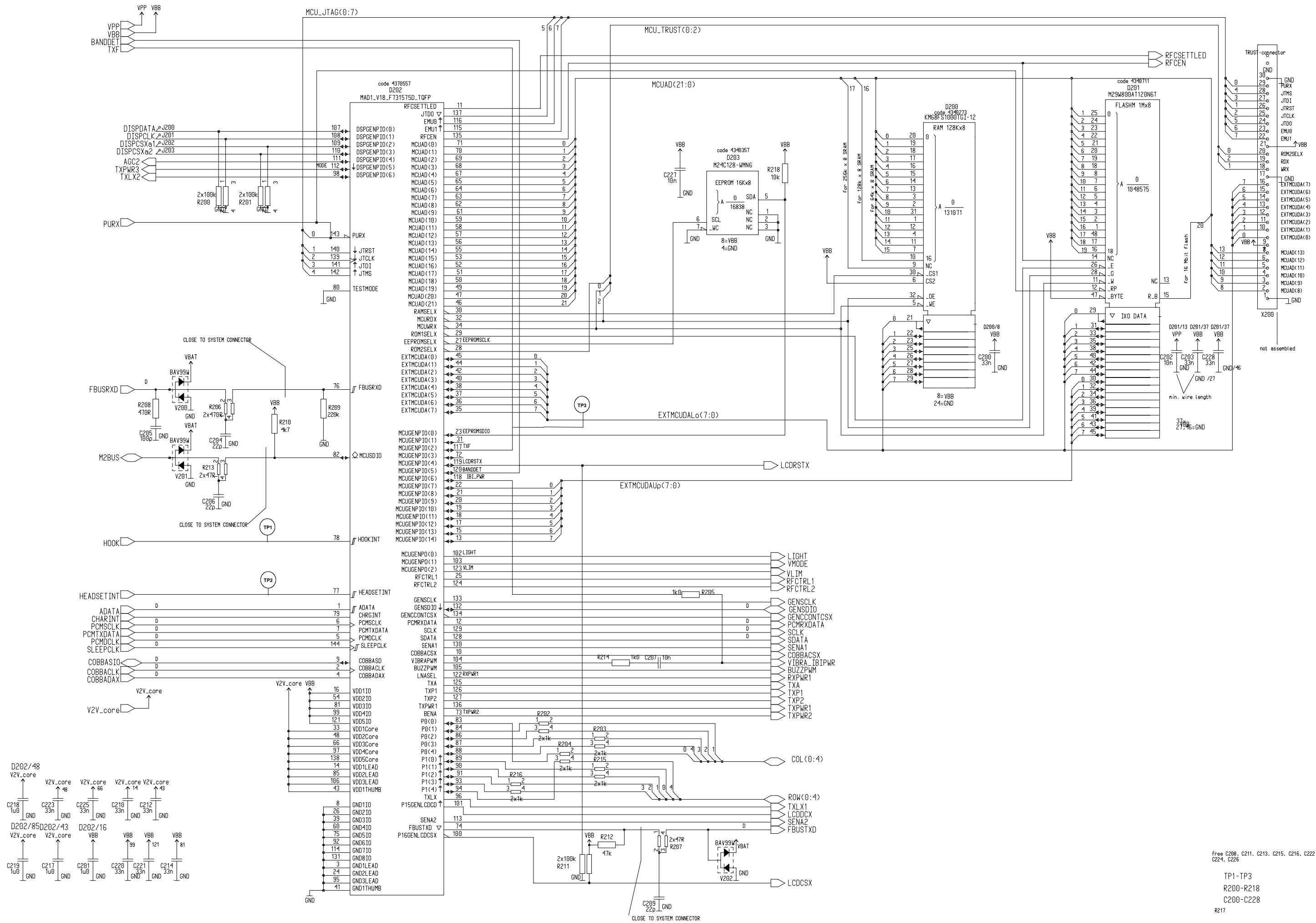


Del file R170, assembled with 2 V MAD core voltage
 Del file C155, not assembled

Free R151, R155, R157, R158, R160
 TP4-TP20
 R150-R170
 C150-C190

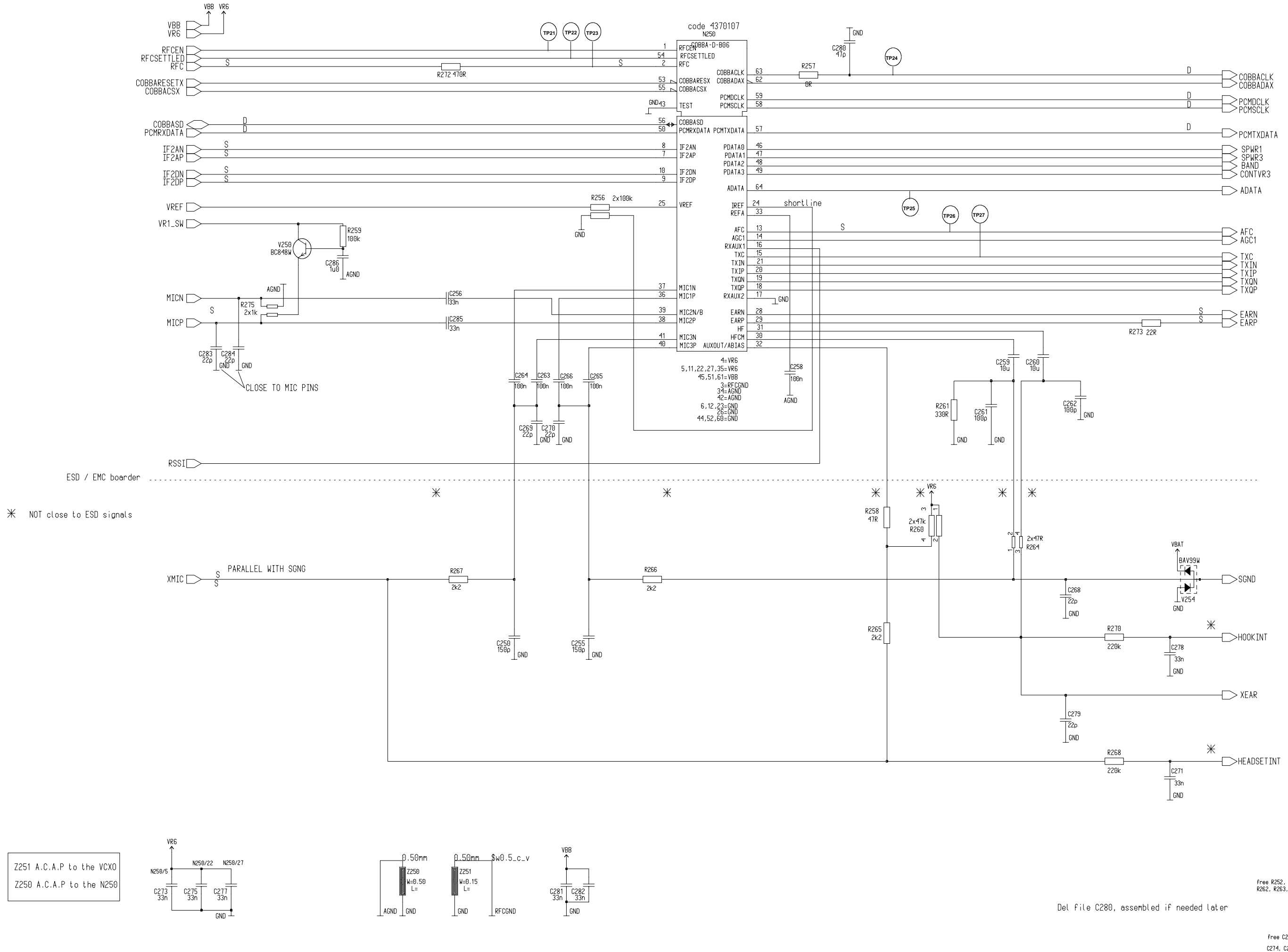
Free C152, C153, C156, C160
 C168, C181, C182, C183, C184, C186.

Circuit Diagram of CTRLU Block (Version 06.43 Edit 10)

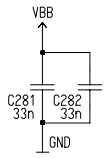
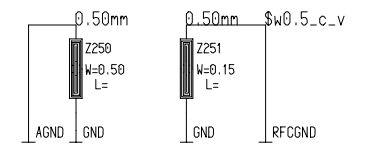
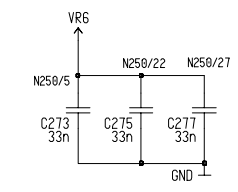


Free C208, C211, C213, C215, C216, C222, C224, C226
 TP1-TP3
 R200-R218
 C200-C228
 R217

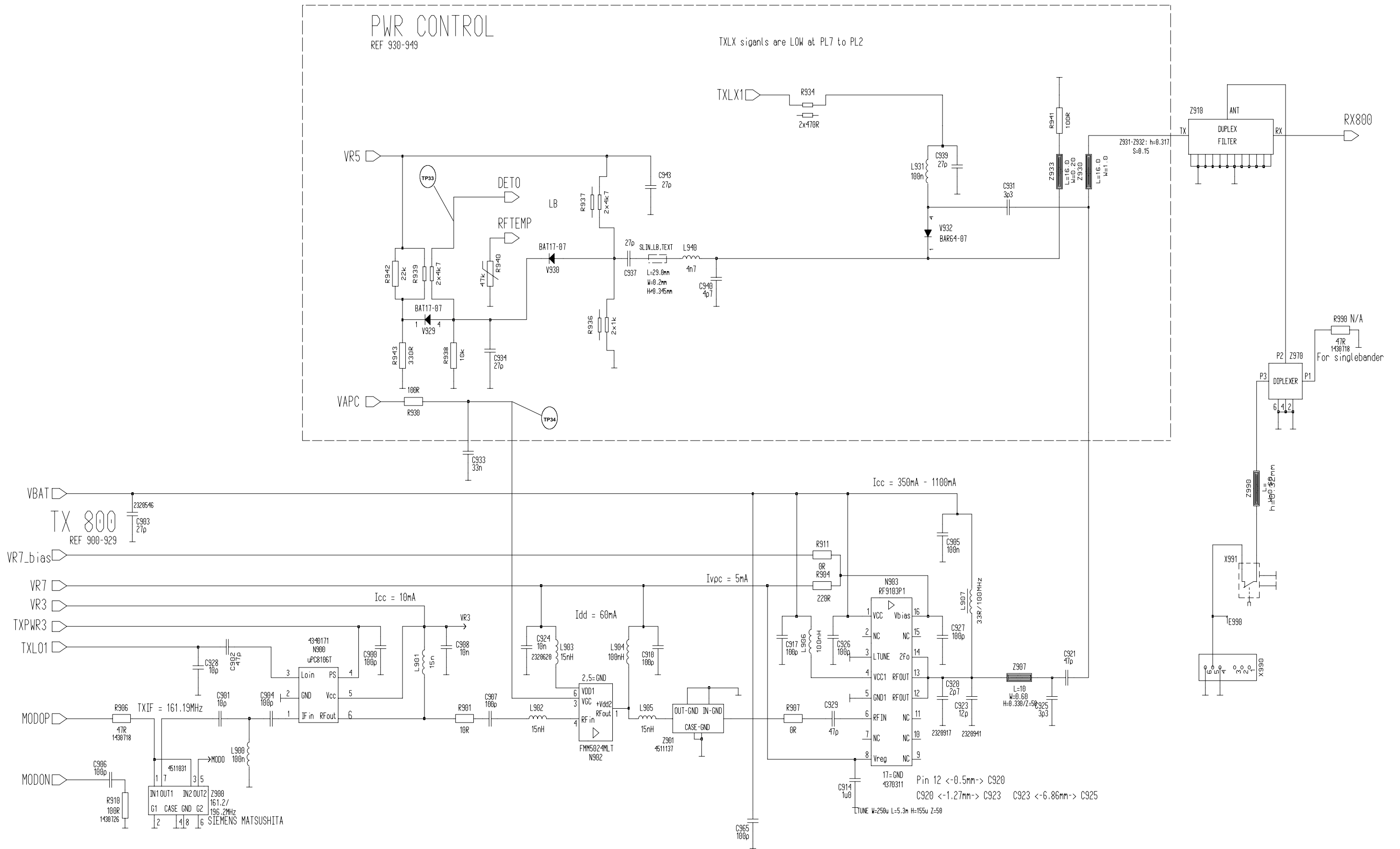
Circuit Diagram of Audio (Version 06.43 Edit 7)

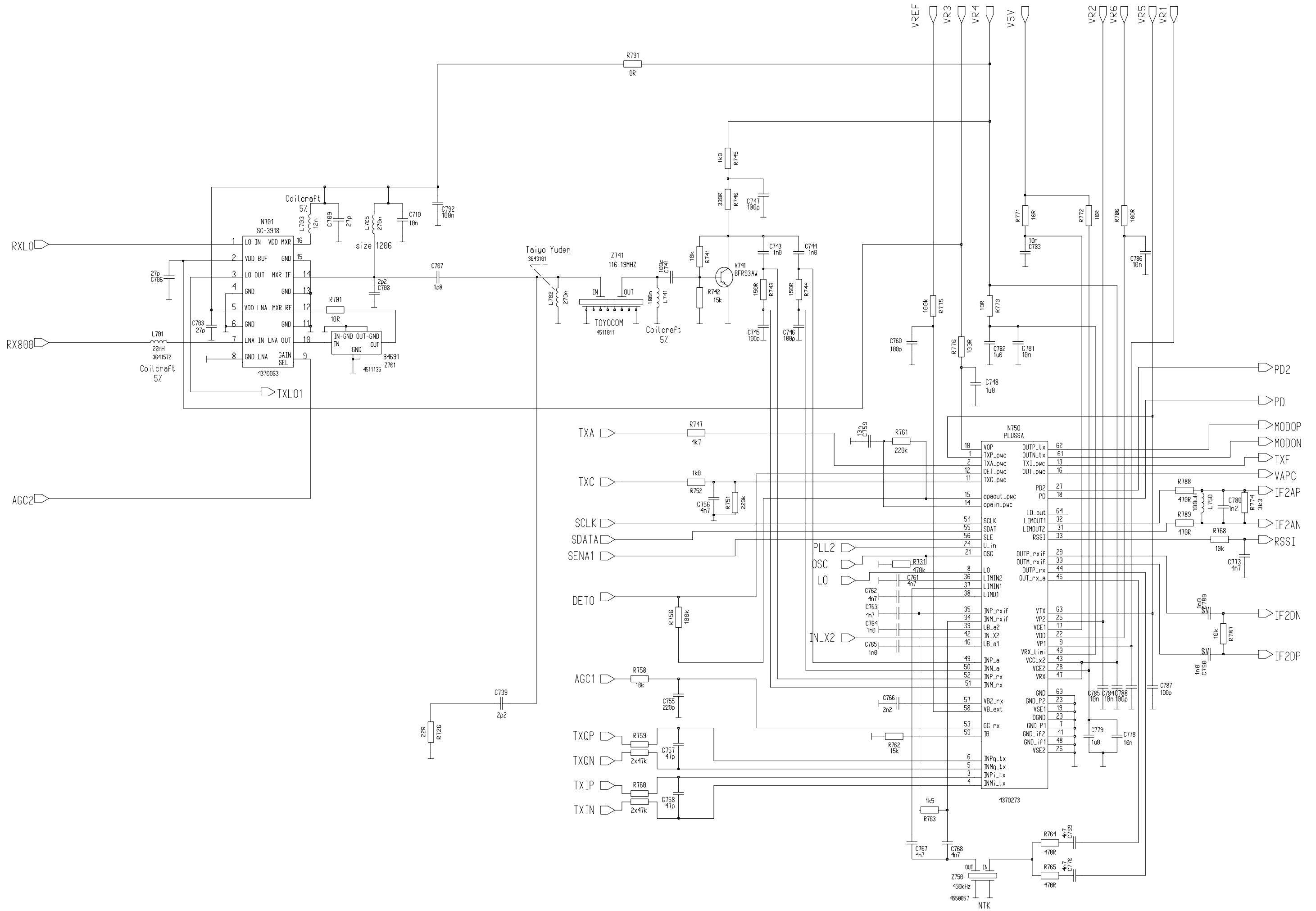


Z251 A.C.A.P to the VCX0
Z250 A.C.A.P to the N250

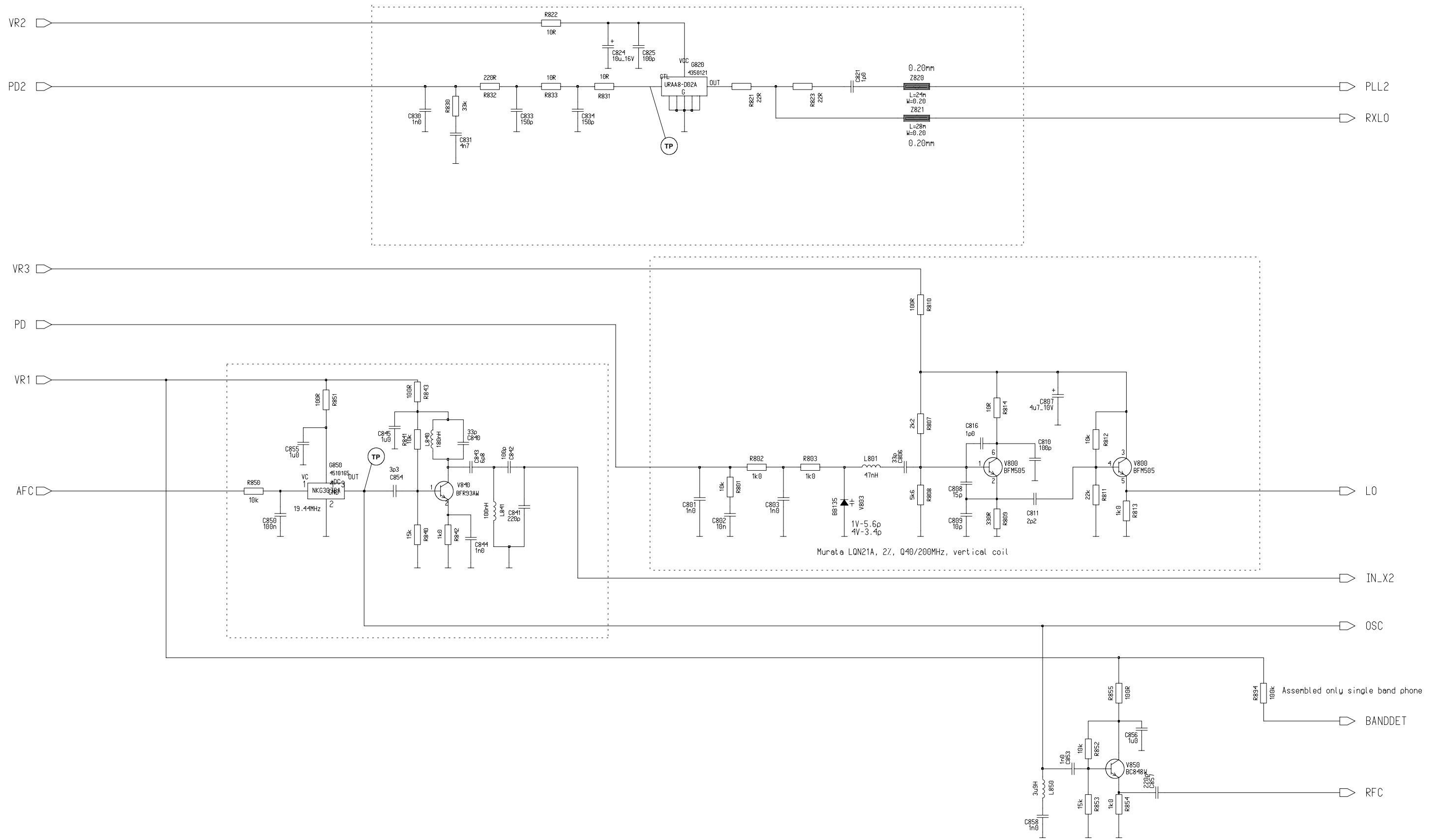


Free R252, R253, R254, R255
R262, R263, R269, R271, R274
TP21-TP27
R252-R275
C250-C286
Free C251, C252, C253, C254, C257
C274, C276

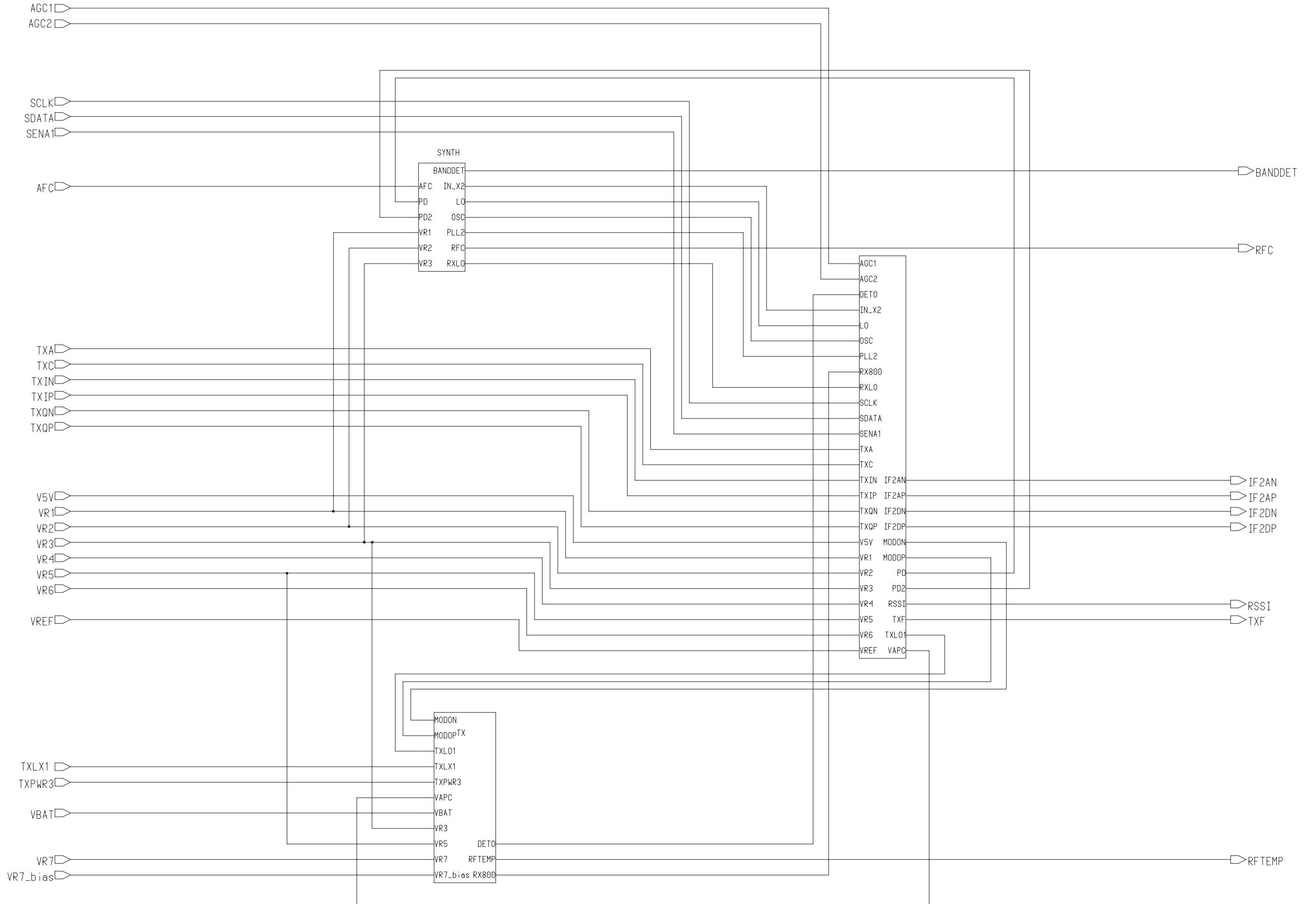


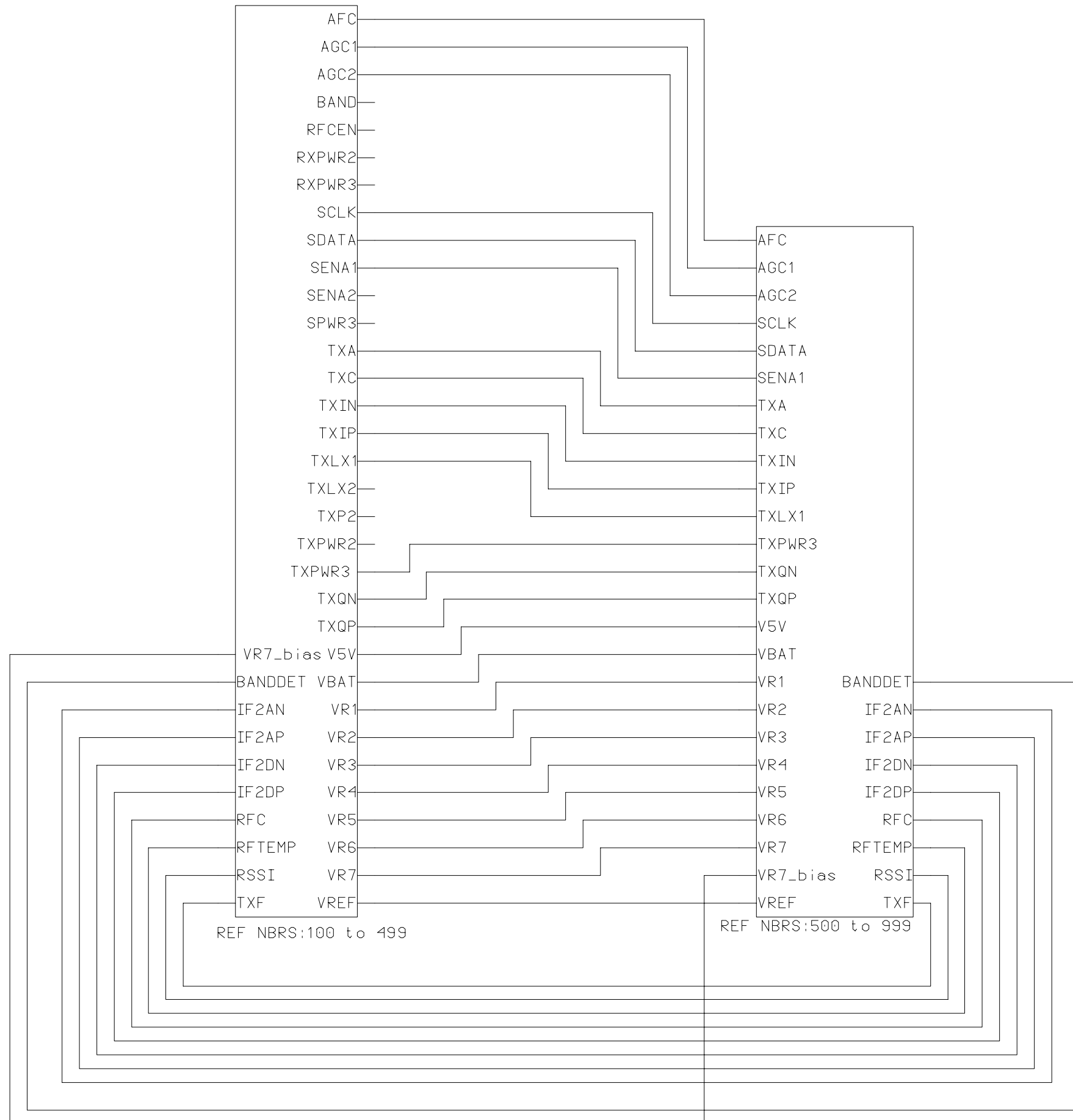


Circuit Diagram of Synthesizer (Version 06.43 Edit 6)

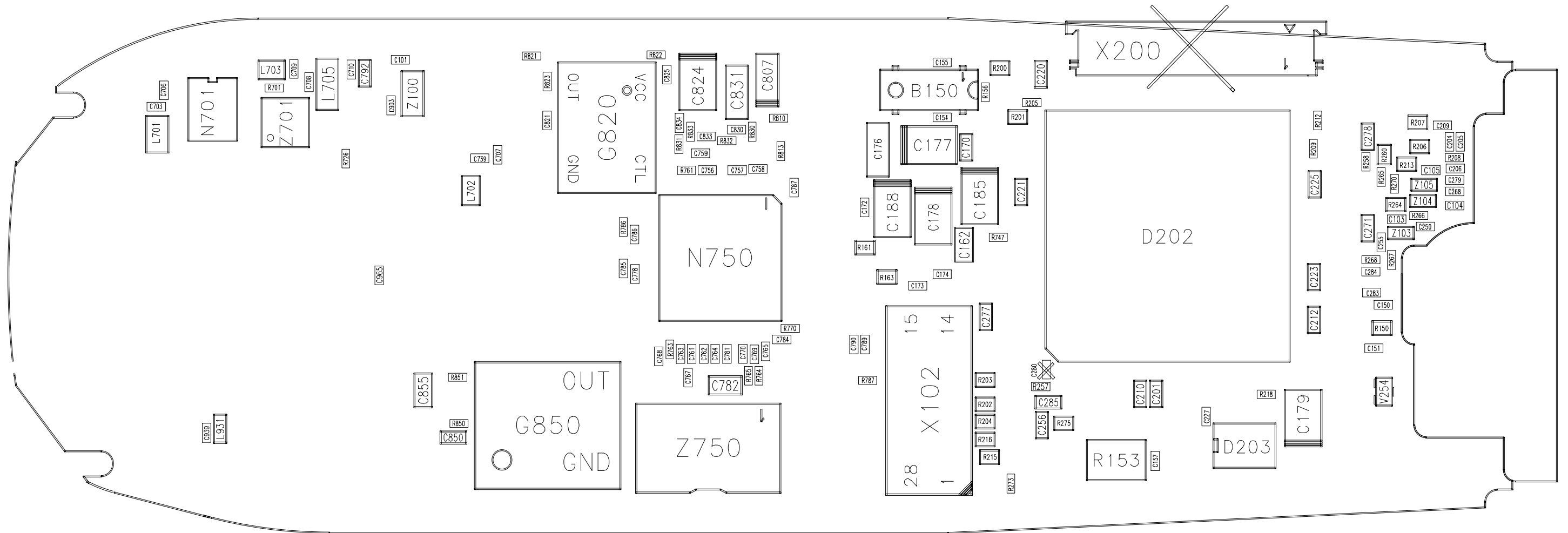


Circuit Diagram of RF Block (Version 06.43 Edit 4)



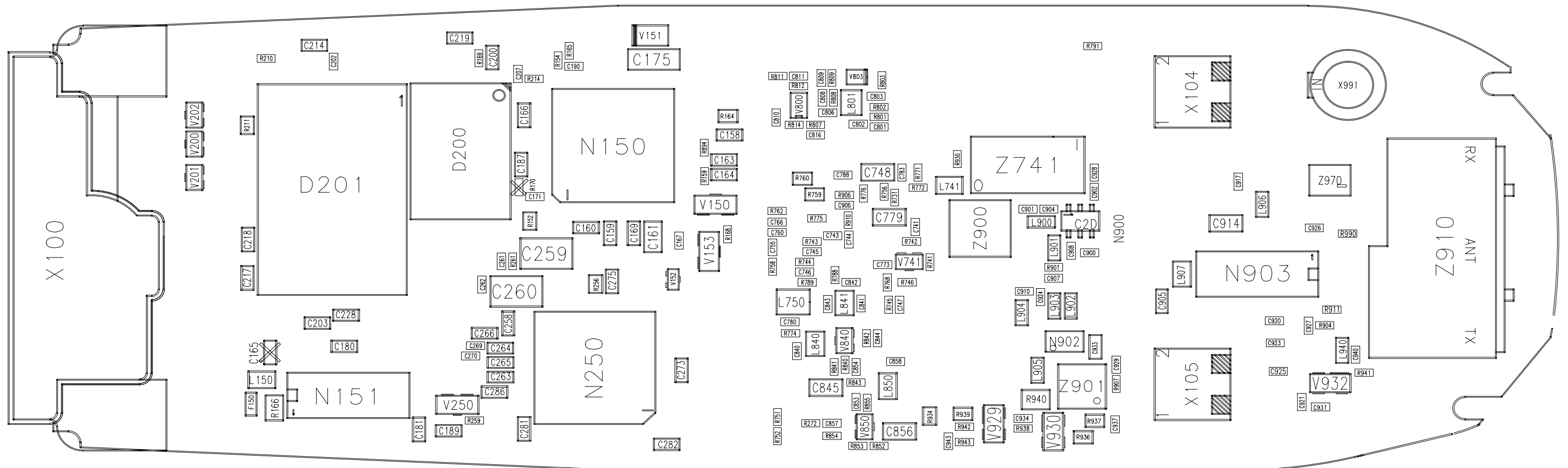


Layout Diagram 1/2 of US4RSM (Layout version 06)



testpoint	name	condition	dc-level	ac-level
J200		Only for R&D use		
J201		Only for R&D use		
J202		Only for R&D use		
J203		Only for R&D use		
TP1, D202 pin 78	HOOKINT	Remote controlheadset	pulse active 2.8 V, non-active 0 V	
TP2, D202 pin 77	HEADSE-TINT	Headset connected	pulse active 0 V, non-active 2.8 V	
TP3, D202 pin 117	TXF	False transmission indicator	Irregular from 0 V to 2.8 V	
TP4, R153	RSense	VOUT detection	min 0V, typ 3.6 V, max 5.2 V	
TP5, R153	VOUT	VOUT detection	min 0V, typ 3.6 V, max 5.2 V	
TP30, G850 pin 3	VCTCXO	power on		typ. 0.8 V – 1.2 Vpp sinwave 19.44 MHz
TP31, G820 pin 3	CTL	active state ch 300	typ. 2.2 V	
TP32, G860 pin 3	CTL	active state ch 1000	typ. 2.2 V	

NOTE: Layout diagram has also upper band (TDMA1900) components included, which are not in actual US4U PCB. Notice this also in testpoints.



testpoint	name	condition	dc-level	ac-level
TP6, N150 pin 11	VR5	supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP7, N150 pin 15	VR4	regulated supply for RX	2.8 V min 2.7 V / max 2.85 V	
TP8, N150 pin 4	VR3	regulated supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP9, N150 pin 9	VR2	regulated supply for SYNT	2.8 V min 2.7 V / max 2.85 V	
TP10, N150 pin 25	VR1	regulated supply for VCTCXO	2.8 V min 2.7 V / max 2.85 V	
TP11, N150 pin 20	VR7	regulated supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP12, N150 pin 19	VR7BASE	VR7 regulator external transistor base current	2.8 V min 2.7 V / max 2.85 V	
TP13, N150 pin 13	VREF	ref.voltage for N150	1.5 V +/- 1.5%	
TP14, N150 pin 55	VBB	regulated supply for BaseBand	2.8 V min 2.7 V / max 2.85 V	
TP15, N150 pin 22	VR6	regulated supply for COBBA	2.8 V min 2.7 V / max 2.85 V	
TP16, N150 pin 32	V5V	regulated supply to 2GHz PLL	5.0 V min 4.8 V / max 5.2 V	
TP17, N150 pin 36	VSIM	regulated supply for flashing	3.0 V min 2.8 V / max 3.2 V	
TP18, N150 pin 54	PURX	RESET Power up/down	reset state 0 V, normal state 2.8 V	

testpoint	name	condition/type	dc-level	ac-level
TP19, N150 pin 52	CCON-TINT	Charger interrupt	pulse active 2.8 V, non-active 0 V	
TP20, N150 pin 48	SLCLK	32.768 kHz, power on	pulsed DC (0V/2.8 V)	
TP21, N250 pin 1	RFCEN	active state	pulse active 2.8 V, non-active 0 V	
TP22, N250 pin 54	RFCSETTLED	active state	pulse active 2.8 V, non-active 0 V	
TP23, N250 pin 2	RFC	19.44 MHz sine-wave		0.2Vpp-1V pp sine-wave
TP24, N250 pin 63	COB-BACKLCK	9.72 MHz, active state	pulsed DC (0V/2.8V)	
TP25, N250 pin 64	ADATA	active state	pulsed DC (0V/2.8V)	
TP26, N250 pin 13	AFC	Autom.Freq.control	0 - 2.3 V, typ. 1.15 V (room temp)	
TP27, N250 pin 15	TXC	TX power control voltage	@level 10 typ.ca 0.5 V pulse @level 2 typ.ca 1.7 V pulse	
TP33, R939	DETO	active state	0.4 V - 2.2 V	
TP34, R220	VAPC	active state	0 V - 1.5 V typ.	
TP35, N702 pins 9,11,12,13,14	VR8 - VR 12	power on	nominal 2.8 V	

NOTE: Layout diagram has also upper band (TDMA1900) components included, which are not in actual US4U PCB. Notice this also in testpoints.